



Endicott Research Group, Inc.

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K3323F



Specifications and Applications Information

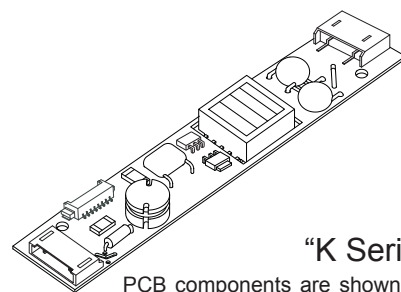
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The ERG K3323F (*8m Class*) low profile dc to ac inverter is specifically designed to power the Kyocera TCG075VG2AA-G00 and TCG075VG2AD-G00 LCD display backlights to a moderate brightness level from a +5 volt dc source.

This low profile inverter features:

- ✓ Less Than 8 mm in Height
- ✓ LCD Module Specific
- ✓ Display Compatible Output Connector
- ✓ Firm Specifications
- ✓ Application Information
- ✓ Designed, Manufactured and Supported in the USA
- ✓ Custom Input and Output Voltages
- ✓ Flexible System Interface
- ✓ Notebook Display Head Compatible

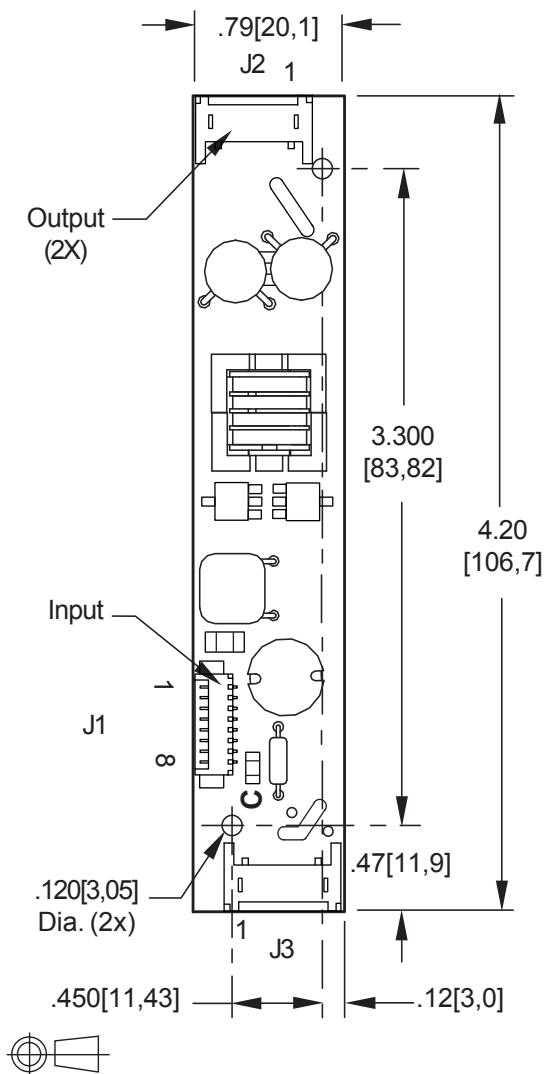
8m Class
2 Lamp
DC to AC Inverter



"K Series" Package

PCB components are shown for reference only. Actual product may differ from that shown.

Package Configuration



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Connectors

Input Connector	Output Connectors
Molex 53261-0871	JST SM02(8.0)B-BHS-1-TB
J1-1 +Vin J1-2 +Vin J1-3 GND J1-4 GND J1-5 Enable/PWM * J1-6 N/C J1-7 N/C J1-8 N/C	J2-1 ACout J2-2 ACreturn J3-1 ACout J3-2 ACreturn
* Valid only with "C" jumper (JP1) removed	

Absolute Maximum Ratings

Rating	Symbol	Value	Units
Input Voltage Range	V_{in}	-0.3 to +5.5	Vdc
Storage Temperature	T_{stg}	-40 to +85	°C

Operating Characteristics

With a load simulating the referenced display and lamp warm-up of 5 minutes.
Unless otherwise noted $V_{in} = 5.00$ Volts dc and $T_a = 25^{\circ}\text{C}$.

Characteristic	Symbol	Min	Typ	Max	Units
Input Voltage	V_{in}	+4.50	+5.00	+5.25	Vdc
Component Surface Temperature ^(note 1)	T_s	-20	-	+80	°C
Input Current ^(note 2)	I_{in}	-	1.13	1.30	Adc
Operating Frequency	F_o	43	48	53	kHz
Minimum Output Voltage ^(note 3)	$V_{out}(\text{min})$	1500	-	-	Vrms
Efficiency	η	-	75	-	%
Output Current (per lamp)	I_{out}	-	5.2	-	mArms
Output Voltage	V_{out}	-	410	-	Vrms
Enable Pin Input Current Requirement ^(notes 4,5,6)	I_{Enable}	-	9	-	mAdc

Specifications subject to change without notice.

(Note 1) Surface temperature must not exceed 80 degrees C; thermal management actions may be required.

(Note 2) Input current in excess of maximum may indicate a load/inverter mismatch condition, which can result in reduced reliability. Please contact ERG technical support.

(Note 3) Provided data is not tested but guaranteed by design.

(Note 4) Required User Enable/Disable Interface Circuit is shown on page 3.

(Note 5) Valid only with "C" jumper (JP1) removed.

(Note 6) With the inverter powered and JP1 is in place, a ground applied to the enable pin J1-5 will open the inverter fuse.

Application Notes:

- 1) The minimum distance from high voltage areas of the inverter to any conductive material should be .12 inches per kilovolt of starting voltage.
- 2) Mounting hardware to be non-conductive.
- 3) Open framed inverters should not be used in applications at altitudes over 10,000 feet.
- 4) ACreturn should be left floating, not grounded.
- 5) Contact ERG for possible exceptions.



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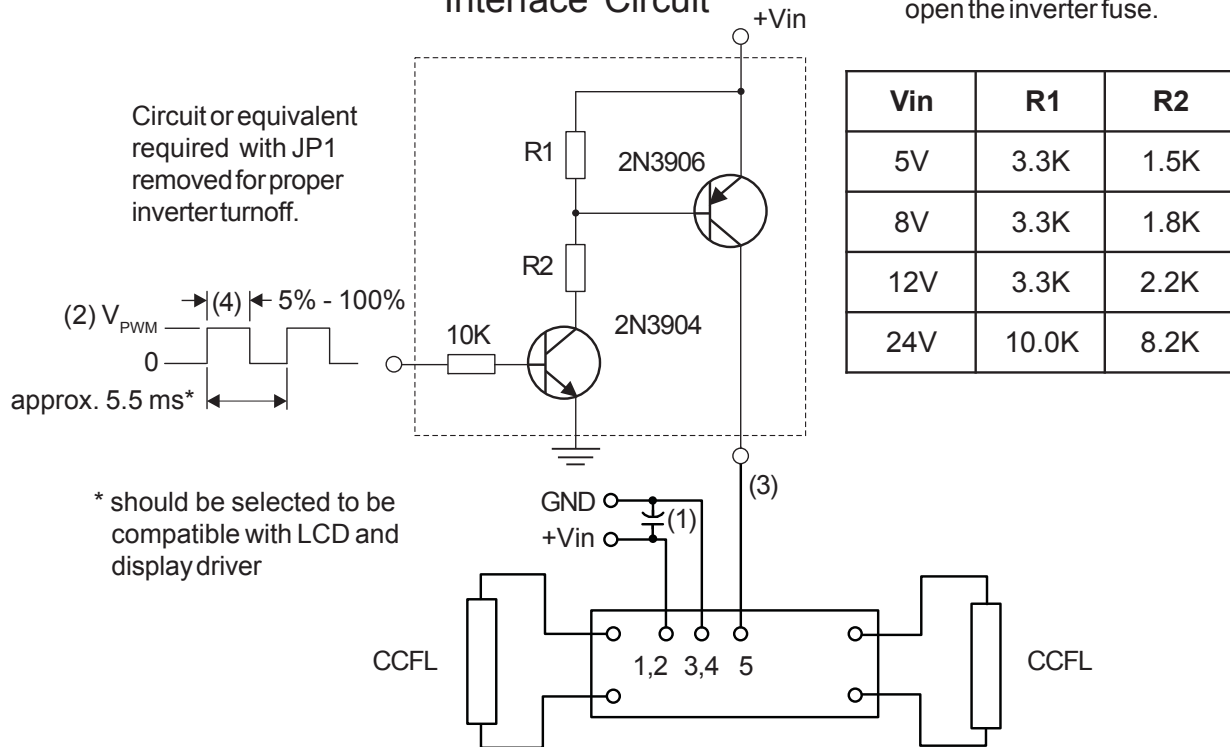
Made in USA



PWM Dimming (Valid only with JP1 removed)

Required User Enable/Disable Interface Circuit

With JP1 in place, a ground applied to the enable pin J1-5 will open the inverter fuse.



- (1) Low ESR type input by-pass capacitor (22 μ F - 100 μ F) may be required to reduce reflected ripple.
- (2) V_{PWM} from 2.4V to less than or equal to $+V_{in}$.
- (3) Full brightness without PWM control requires that pin 5 be tied to $+V_{in}$. Pin 5 must be at 0V to turn off.
- (4) Duty Cycle 5% - 100%.



Endicott Research Group, Inc. (ERG) reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by ERG is believed to be accurate and reliable. However, no responsibility is assumed by ERG for its use.