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Specifications and Applications Information

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The ERG *Smart Force Series* of LED Drivers are specifically designed for applications which require high efficiency, wide dimming and LCD brightness stability over a wide input voltage range. The SFDZDB4220F is designed to provide backlight power for the Optrex T55592D121J-LW-A-ABN display.

Designed, manufactured and supported within the USA, the SFDZD features:

- ✓ Constant LED current
- ✓ High efficiency
- ✓ On-board PWM dimming
- ✓ High dimming ratio
- ✓ Separate enable and dimming function
- ✓ Open/short circuit protection
- ✓ Soft start
- ✓ One year warranty

Connectors

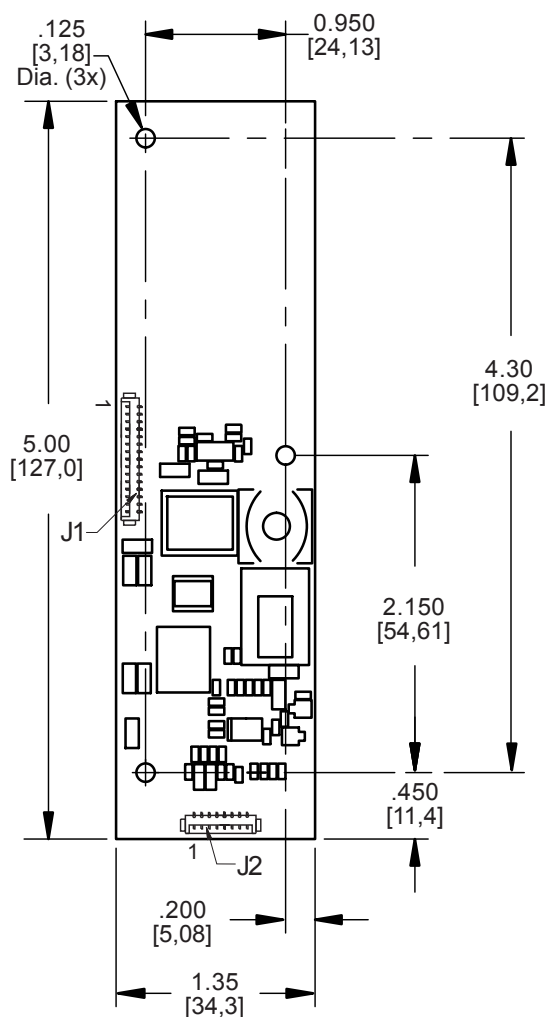
Input Connector	Output Connector *
Molex 53261-1571	Molex 53261-0871
J1-1,2,3 Vin(+) J1-4,5,6 Vin(+) J1-7,8,9 GND J1-10,11,12 GND J1-13 Enable J1-14 N/C J1-15 Control	J2-1 Cathode 1 J2-2 Anode 1 J2-3 Cathode 2 J2-4 Anode 2 J2-5 Cathode 3 J2-6 Anode 3 J2-7 Cathode 4 J2-8 Anode 4
* Requires harness: ERG part number H13208152F recommended	

SFDZDB4220F



Smart Force LED Driver

Package Configuration



Mass: 35 grams



**Absolute Maximum Ratings**

Rating	Symbol	Value	Units
Input Voltage Range	V_{in}	-0.3 to +20	Vdc
Storage Temperature	T_{stg}	-40 to +85	°C
Control Voltage	$V_{Control}$	0 to 6.0	Vdc
Enable Input Voltage	V_{Enable}	0 to 6.0	Vdc

Operating Characteristics

Unless otherwise noted $V_{in} = 12.00$ Volts dc and $T_a = 25^{\circ}\text{C}$.

Characteristic	Symbol	Min	Typ	Max	Units
Input Voltage	V_{in}	+10.8	+12.0	+18.0	Vdc
Component Surface Temperature (Note 1)	T_s	-20	-	+80	°C
Input Current (Note 2)	I_{in}	0.82	0.97	1.12	Adc
LED String Voltage	V_{LED}	20	-	30	Vdc
Efficiency (Note 2)	η	-	93	-	%
Output Current (per string)	I_{out}	100	105	110	mArms
Enable Pin					
Turn-on Threshold (Note 3)	V_{thon}	-	-	1.8	Vdc
Turn-off Threshold	V_{thoff}	0.6	-	-	Vdc
Enable Input Impedance (Note 4)	R_{Enable}	-	8.5	-	kOhms
Control Pin (Notes 5,6)					
Full-on Threshold	V_{fon}	-	1.0	-	Vdc
Minimum Pulse Width Threshold	V_{PWmin}	-	4.5	-	Vdc

Specifications subject to change without notice.

- Note 1 Surface temperature must not exceed 80°C ; thermal management actions may be required.
- Note 2 Input Current and Efficiency are calculated with 25.9V LED strings.
- Note 3 Enable pin is internally pulled up above the Turn-on Threshold.
- Note 4 Enable pin input impedance is $8.5\text{k}\Omega$ to 3V with a 12V input voltage.
- Note 5 Internally pulled to GND.
- Note 6 Control pin input impedance is 485 kohm.



Onboard PWM

Unless otherwise noted $V_{in} = 12.00$ Volts DC, $T_a = 25$ °C and unit has been running for 5 minutes.

Characteristic	Symbol	Min	Typ	Max	Units
Frequency	f_{pwm}	-	245	-	Hz
Control Input Bias Current	I_{cbias}	-	-	10	μA

Application Information

The ERG SFDZDB4220F has been designed to be configured in multiple ways:

NO DIMMING

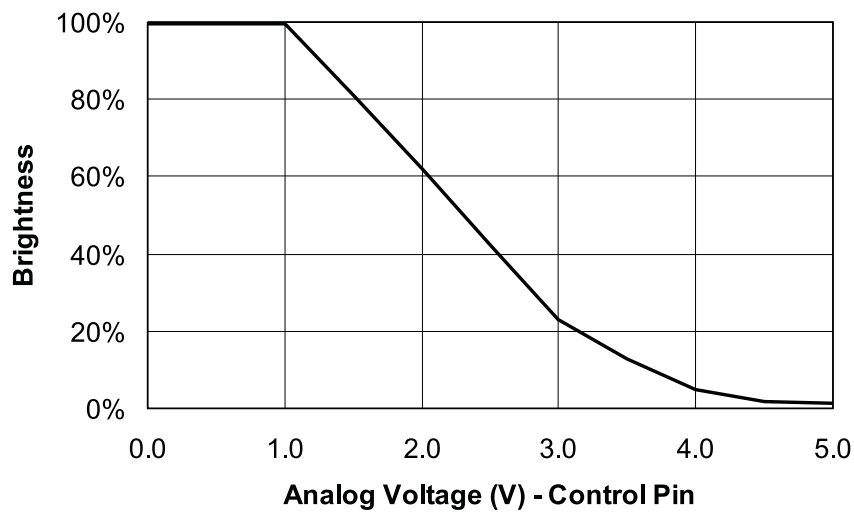
- OPERATION: The SFD driver can be configured to operate without dimming by floating the Control Pin (J1-15) and the Enable Pin (J1-13).
- Pins 1 through 6 of connector J1 must be connected to +Vin, between 10.8 and 18 Vdc. Pins 7 through 12 of connector J1 must be connected to GND.

ONBOARD PWM DIMMING

- OPERATION: Onboard PWM configuration as shown in Figure 1 allows the user to control display brightness by controlling the onboard PWM generator. The user is responsible to provide an analog control signal. A dimming ratio up to 255:1 is possible with this configuration.
- DIMMING: Dimming is accomplished by applying an analog voltage to the Control Pin (J1-15). Display brightness is modulated by controlling the Control Pin voltage as shown in Graph 1.
- ENABLE/DISABLE: The driver may be enabled or disabled (turned on and off) by applying a DC voltage to the Enable Pin(J1-13). Enable Pin on and off levels are specified in the Operating Characteristics section of the data sheet. The driver can also be enabled by floating the Enable Pin.
- Pins 1 through 6 of connector J1 must be connected to +Vin, between 10.8 and 18 Vdc. Pins 7 through 12 of connector J1 must be connected to GND. Pin 14 may be left floating or pulled up.



ONBOARD PWM DIMMING



Graph 1

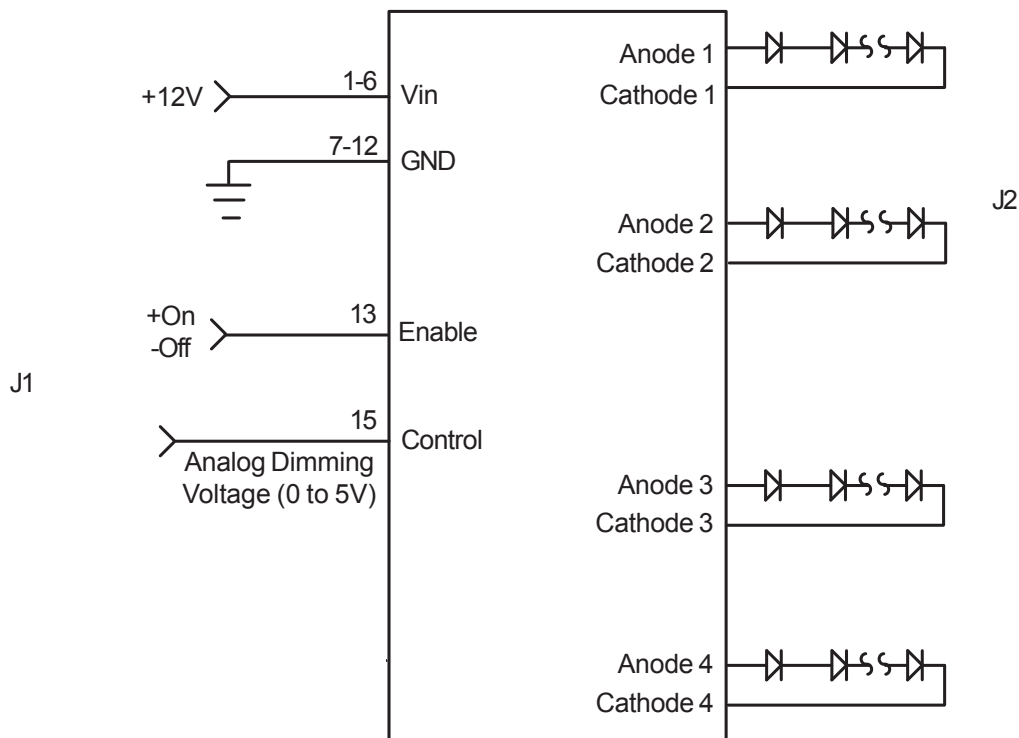


Figure 1



Endicott Research Group, Inc. (ERG) reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by ERG is believed to be accurate and reliable. However, no responsibility is assumed by ERG for its use.