



Endicott Research Group, Inc.

2601 Wayne St., Endicott, NY 13760
607-754-9187 Fax 607-754-9255
http://www.ergpower.com

SFDQDB4406F



Specifications and Applications Information

12/16/15

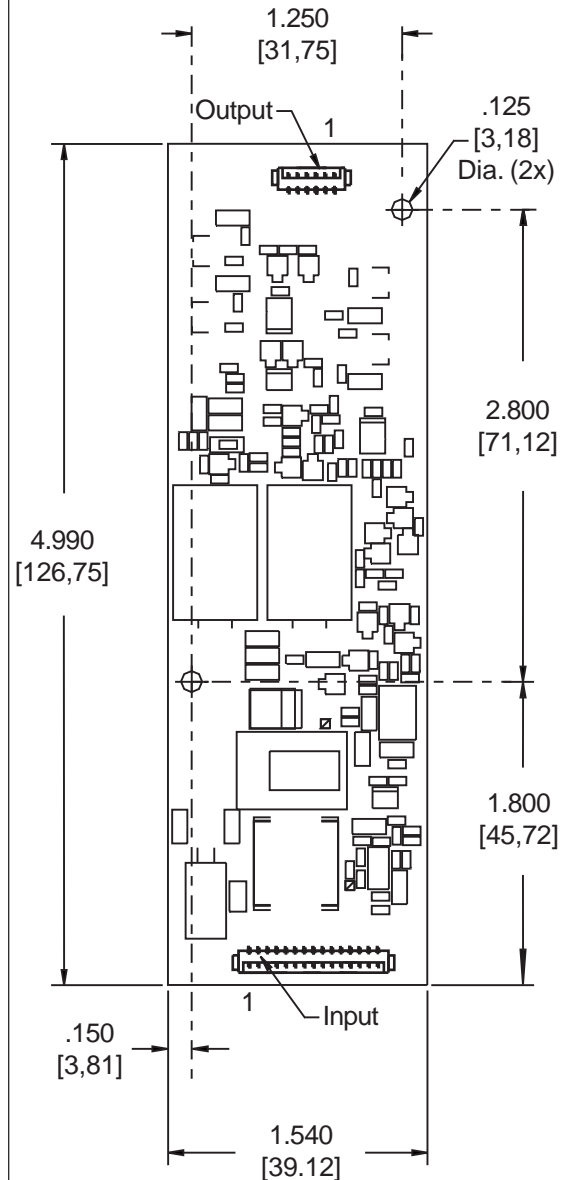
Smart Force LED Driver

The ERG *Smart Force Series* of LED Drivers are specifically designed for applications which require wide dimming and LCD brightness stability over a wide input voltage range. The SFDQDB4406F is designed to provide backlight power for the AU Optronics G238HAN01.0 display.

Designed, manufactured and supported within the USA, the SFDQD features:

- ✓ Wide input voltage range
- ✓ Constant LED current
- ✓ External dimming or on-board dimming
- ✓ High dimming ratio
- ✓ Soft start
- ✓ One year warranty

Package Configuration



PCB components are shown for reference only. Actual product may differ from that shown.

Mass: 34 grams typ.



Connectors

Input Connector		Output Connector *	
Molex 53261-1571		Molex 53261-0871	
J1-1,2,3	Vin(+)	J2-1	Cathode 1
J1-4,5,6	Vin(+)	J2-2	Anode 1
J1-7,8,9	GND	J2-3	Cathode 2
J1-10,11,12	GND	J2-4	Anode 2
J1-13	N/C	J2-5	Cathode 3
J1-14	Enable	J2-6	Anode 3
J1-15	Control	J2-7	Cathode 4
		J2-8	Anode 4

* Requires harness:
ERG part number H18606152F recommended

**Absolute Maximum Ratings**

Rating	Symbol	Value	Units
Input Voltage Range	V_{in}	-0.3 to +20.0	Vdc
Storage Temperature	T_{stg}	-40 to +85	°C
Enable Input Voltage	V_{Enable}	0 to V_{in}	Vdc
Control Input Voltage	V_{PWM}	0 to +5.0	Vdc

Operating Characteristics

Unless otherwise noted $V_{in} = 12.00$ Volts dc and $T_a = 25^{\circ}\text{C}$.

Characteristic	Symbol	Min	Typ	Max	Units
Input Voltage	V_{in}	+10.8	+12.0	+18.0	Vdc
Component Surface Temperature (Note 1)	T_s	-40	-	+80	°C
Peak Inrush Current (Note 2)	I_{peak}	-	2.3	-	Adc
Input Current	I_{in}	1.23	1.47	1.67	Adc
LED String Voltage	V_{LED}	48.0	-	61.5	Vdc
Efficiency (Note 3)	η	-	87	-	%
Output Current (per string)	I_{out}	66	69	72	mAdc
Enable Pin (Note 4)					
Turn-on Threshold	V_{thon}	-	-	2.0	Vdc
Turn-off Threshold	V_{thoff}	0.8	-	-	Vdc
Enable Input Impedance (Note 5)	R_{Enable}	-	10	-	kOhms
Control Pin (Notes 6,7)					
Full-on Threshold	V_{thon}	-	1.0	-	Vdc
Full-off Threshold	V_{thoff}	-	4.5	-	Vdc
Control Input Bias Current	I_{Cbias}	-	-	10	uA
Frequency	F_{PWM}	-	245	-	Hz

Specifications subject to change without notice.

- Note 1 Surface temperature must not exceed 80°C .
 Note 2 Peak inrush occurs over a 1 to 3 ms time period during initial startup.
 Note 3 Efficiency is calculated using a 55.7V load.
 Note 4 Enable pin is internally pulled up above the turn-on threshold
 Note 5 Enable pin input impedance is $10\text{k}\Omega$ to $12\text{k}\Omega$.
 Note 6 Control pin is internally pulled to GND.
 Note 7 Control pin input impedance is $485\text{k}\Omega$.



Application Information

The ERG SFDQDB4406F has been designed to be configured in multiple ways:

NO DIMMING

- OPERATION: The SFDQ can be configured to operate without dimming by floating the Control (J1-15) pin and Enable (J1-14) pin.
- Pins 1 through 6 of connector J1 must be connected to +Vin, between 10.8 and 18 Vdc. Pins 7 through 12 of connector J1 must be connected to GND.

ONBOARD PWM DIMMING

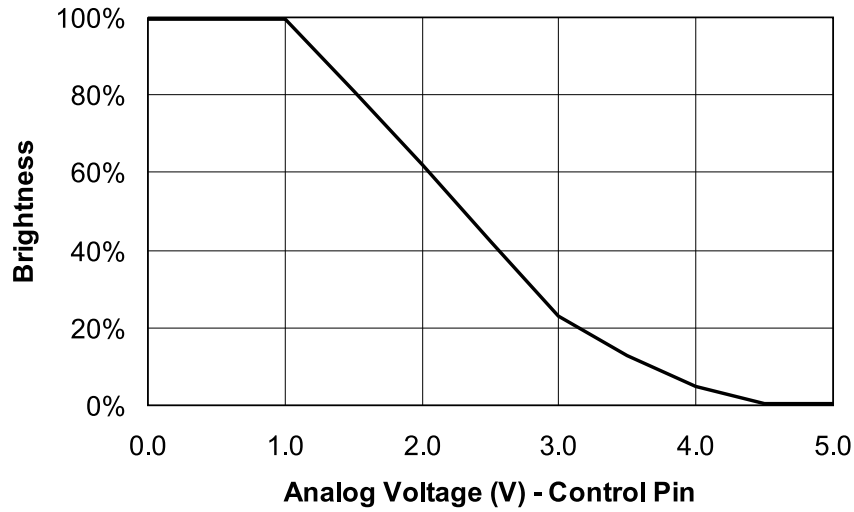
- OPERATION: Onboard PWM configuration as shown in Figure 1 allows the user to control display brightness by controlling the onboard PWM generator. The user is responsible to provide an analog control signal.
- DIMMING: Dimming is accomplished by applying an analog voltage to the Control Pin (J1-15). Display brightness is modulated by controlling the Control Pin voltage as shown in Graph 1.
- ENABLE/DISABLE: The driver may be enabled or disabled (turned on and off) by applying a DC voltage to the Enable Pin (J1-14). Enable Pin on and off levels are specified in the Operating Characteristics section of the data sheet. Enable Pin is internally pulled up above the turn-on threshold.
- Pins 1 through 6 of connector J1 must be connected to +Vin, between 10.8 and 18 Vdc. Pins 7 through 12 of connector J1 must be connected to GND.

EXTERNAL PWM DIMMING

- OPERATION: External PWM configuration as shown in Figure 2 allows the user to control display brightness with an externally generated PWM signal. The user is responsible to provide the PWM signal.
- DIMMING: Dimming is accomplished by applying a PWM signal to the Enable Pin (J1-14). Enable on and off levels are specified in the Operating Characteristics section of the data sheet. Display brightness is modulated by controlling the PWM duty cycle as shown in Graph 2.
- Pins 1 through 6 of connector J1 must be connected to +Vin, between 10.8 and 18 Vdc. Pins 7 through 12 of connector J1 must be connected to GND.
- Control Pin (J1-15) should be left floating or connected to GND.



ONBOARD PWM DIMMING



Graph 1

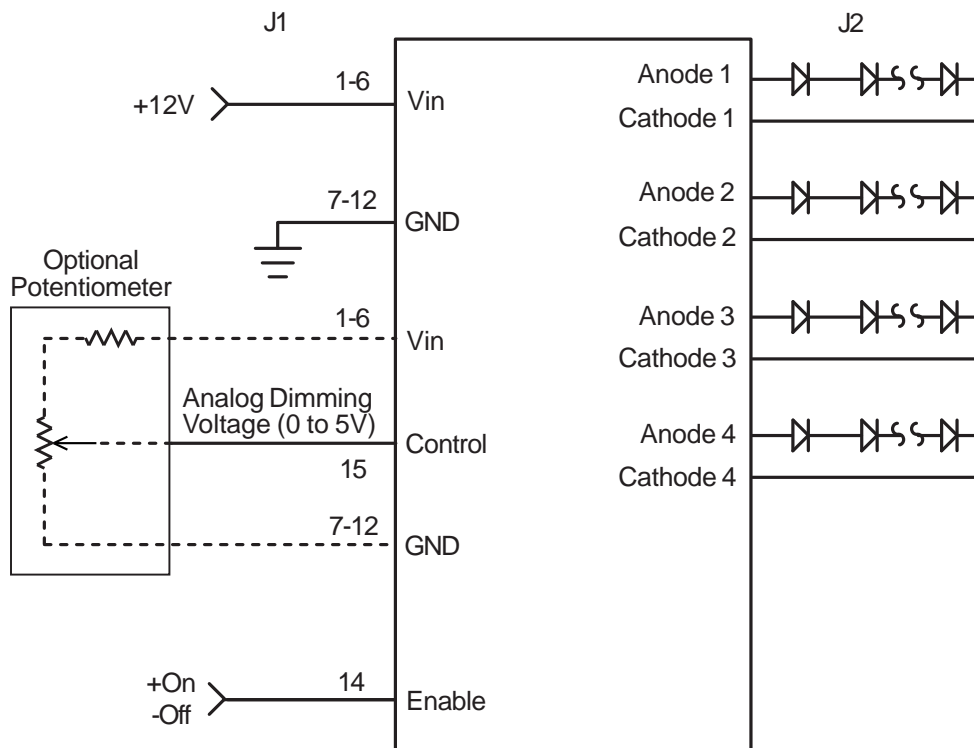
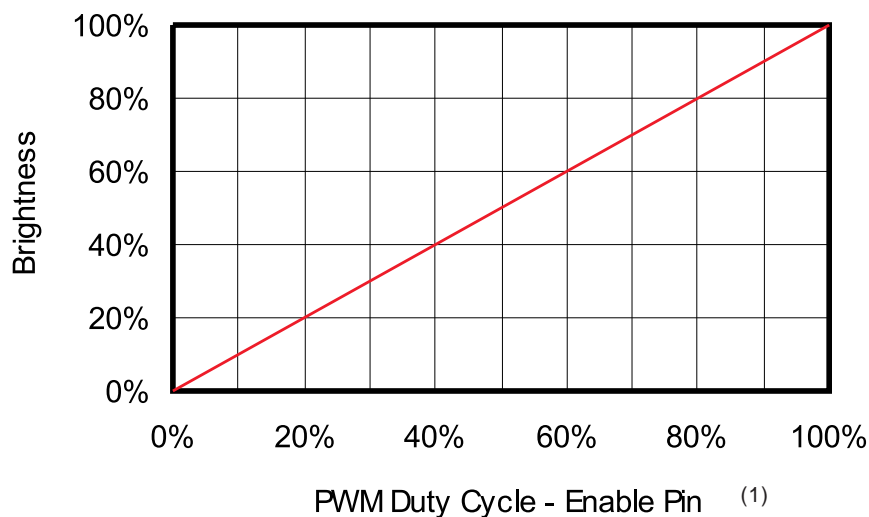


Figure 1



EXTERNAL PWM DIMMING



(1) Nonlinear relationship from 0 to 2% duty cycle.

Graph 2

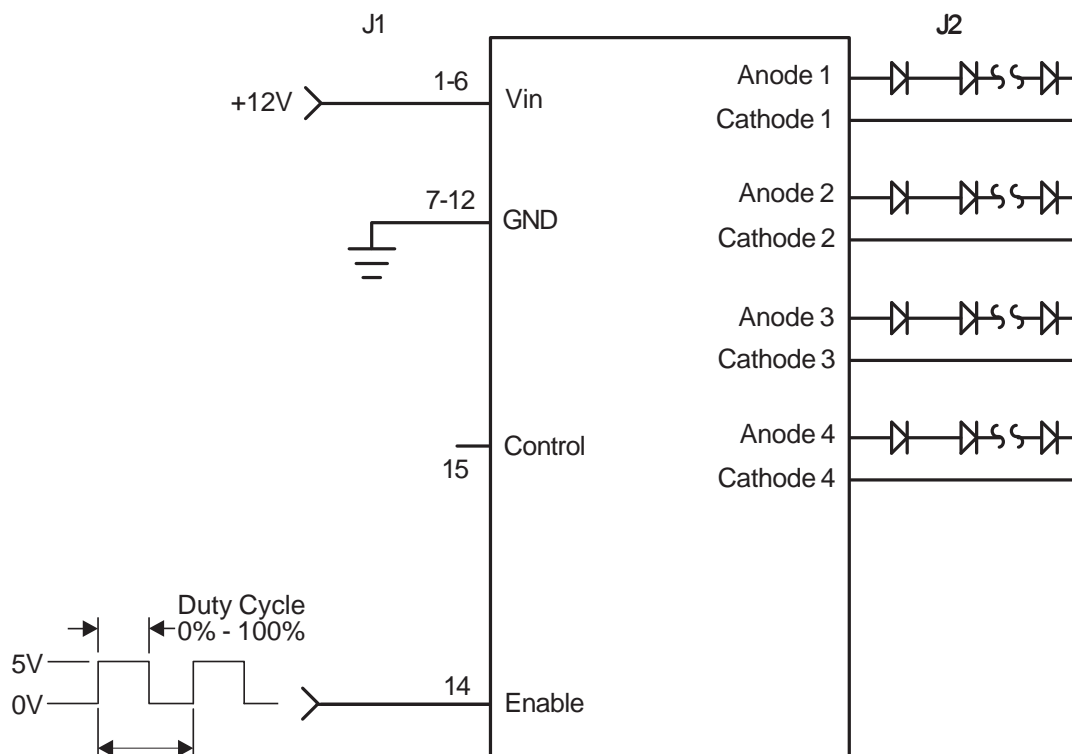


Figure 2



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