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# SFDMDB3983F



## Specifications and Applications Information

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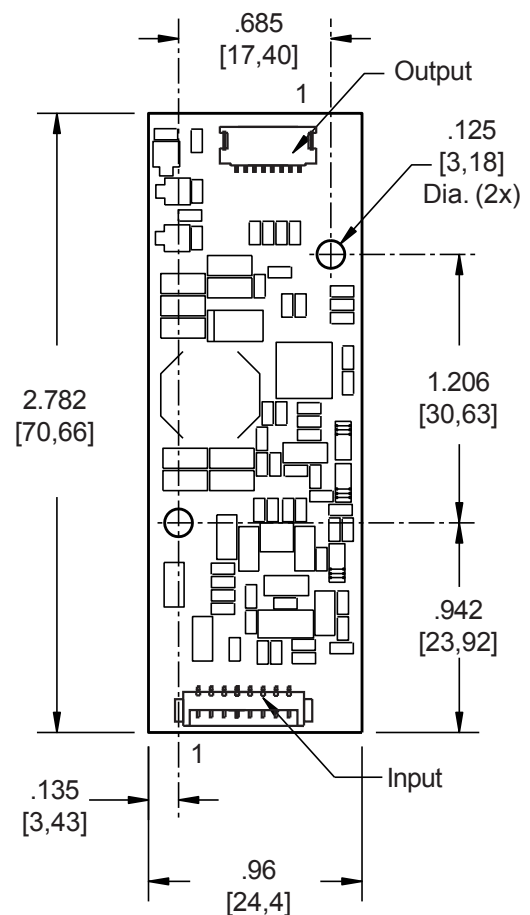
## Smart Force LED Driver

The ERG *Smart Force Series* of LED Drivers are specifically designed for applications which require high efficiency, small footprint and LCD brightness stability over a wide input voltage range. The SFDMDB3983F is designed to provide backlight power for the Kyocera TCG075VGLAE-G00 display.

Designed, manufactured and supported within the USA, the SFDMD features:

- ✓ Less than 5 mm in height
- ✓ Wide input voltage range
- ✓ Constant LED current
- ✓ With internal dimming signal, up to 255:1 dimming ratio
- ✓ Open and short circuit protection
- ✓ High efficiency
- ✓ Separate enable and dimming function
- ✓ Soft start
- ✓ One year warranty

### Package Configuration

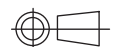


PCB components are shown for reference only. Actual product may differ from that shown.

### Connectors

Input Connector	Output Connector			
Molex 53261-0871	JST SM08B-SHLS-TF			
J1-1 Vin(+)	J2-1 Anode 1	J2-5 Cathode 1		
J1-2 Vin(+)	J2-2 Anode 2	J2-6 Cathode 2		
J1-3 GND	J2-3 Anode 3	J2-7 Cathode 3		
J1-4 GND	J2-4 Anode 4	J2-8 Cathode 4		
J1-5 Enable				
J1-6 N/C				
J1-7 Control				
J1-8 Fault Indicator (output)				

Mass: 9 grams typ.



**Absolute Maximum Ratings**

Rating	Symbol	Value	Units
Input Voltage Range	$V_{in}$	-0.3 to +20.0	Vdc
Storage Temperature	$T_{stg}$	-40 to +85	°C
Enable Input Voltage	$V_{Enable}$	0 to $V_{in}$	Vdc
Control Input Voltage	$V_{PWM}$	0 to +5.0	Vdc
Fault Indicator	$V_{FL}$	0 to +4.0	Vdc

**Operating Characteristics**

Unless otherwise noted  $V_{in} = 12.00$  Volts dc and  $T_a = 25^\circ\text{C}$ .

Characteristic	Symbol	Min	Typ	Max	Units
Input Voltage	$V_{in}$	+8.0	+12.0	+16.0	Vdc
Component Surface Temperature (Note 1)	$T_s$	-40	-	+80	°C
Input Current	$I_{in}$	0.19	0.22	0.25	Adc
LED String Voltage (Note 2)	$V_{LED}$	21.0 (Note 3)	-	38.5	Vdc
Efficiency (Note 4)	$\eta$	-	87	-	%
Output Current (per string)	$I_{out}$	24	25	26	mAdc
<b>Enable Pin</b> (Note 5)					
Turn-on Threshold	$V_{thon}$	-	-	3.5	Vdc
Turn-off Threshold	$V_{thoff}$	0.8	-	-	Vdc
Enable Input Impedance (Note 6)	$R_{Enable}$	-	9.0	-	kOhms
<b>Control Pin</b> (Notes 7,8)					
Full-on Threshold	$V_{thon}$	-	1.0	-	Vdc
Minimum Pulse Width Threshold	$V_{PWmin}$	-	4.5	-	Vdc
Control Input Bias Current	$I_{Cbias}$	-	-	10	uA
Frequency	$F_{PWM}$	-	245	-	Hz

(Operating Characteristics and notes are continued on next page.)



## Operating Characteristics (continued)

Characteristic	Symbol	Min	Typ	Max	Units
<b>Fault Indicator</b>					
No Fault Level (Note 9)	$V_{NFL}$	-	2.5	-	Vdc
Fault Level (Note 9)	$V_{FL}$	-	0.3	-	Vdc

Specifications subject to change without notice.

- Note 1 Surface temperature must not exceed 80°C, except U1, which cannot exceed 95°C.  
Note 2 Exceeding maximum string voltage specification will damage the LED driver.  
Note 3 The LED driver is capable of driving strings less than the minimum string voltage specification, although doing so will limit the maximum input voltage.

To determine max Vin:

$$\text{minimum LED string voltage} \geq (1.3) \times (V_{in \text{ maximum}})$$

- Note 4 Efficiency is calculated using a 23V LED string.  
Note 5 The Enable pin is internally pulled up above the turn-on threshold.  
Note 6 Enable pin input impedance is 9kΩ to 8V with a 12V input voltage.  
Note 7 Control pin is internally pulled up above the turn-on threshold.  
Note 8 Control pin input impedance is 485kΩ.  
Note 9 Loading with an impedance less than 100kΩ to Vcc or to ground may cause the default levels to change.



## Application Information

The ERG SFDMDB3983F has been designed to be configured in multiple ways:

### NO DIMMING

- OPERATION: The SFD can be configured to operate without dimming by floating the Enable (J1-5) and Control (J1-7) pins.
- Pins 1 and 2 of connector J1 must be connected to +Vin, between 8 and 16 Vdc. Pins 3 and 4 of connector J1 must be connected to GND.
- DISABLING DRIVER: Pulling the Enable pin (J1-5) below the minimum turn-off threshold of 0.8V will disable the driver. Disabling the driver will require the ability to sink  $\geq 2\text{mA}$  below the turn-off threshold. This pin may be driven by an open collector stage or a totem pole stage.

### ONBOARD PWM DIMMING

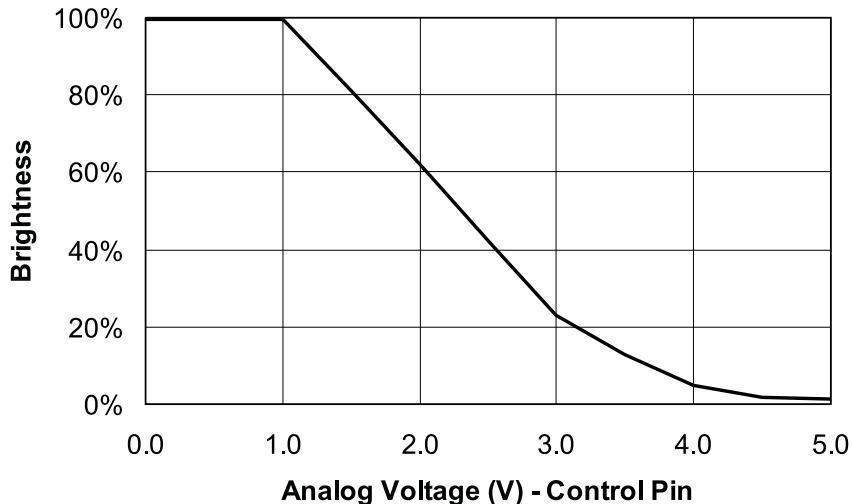
- OPERATION: Onboard PWM configuration as shown in Figure 1 allows the user to control display brightness by controlling the onboard PWM generator. The user is responsible to provide an analog control signal. A dimming ratio up to 255:1 is possible with this configuration.
- DIMMING: Dimming is accomplished by applying an analog voltage to the Control Pin (J1-7). Display brightness is modulated by controlling the Control Pin voltage as shown in Graph 1.
- ENABLE/DISABLE: The driver may be enabled or disabled (turned on and off) by applying a DC voltage to the Enable Pin (J1-5). Enable Pin on and off levels are specified in the Operating Characteristics section of the data sheet. The driver can also be enabled by floating the Enable Pin.
- Pins 1 and 2 of connector J1 must be connected to +Vin, between 8 and 16 Vdc. Pins 3 and 4 of connector J1 must be connected to GND.

### FAULT INDICATOR

- The Fault Indicator pin (J1-8) may be used as a feedback signal that will fall below the fault level of 0.3V in the case of an open string, a shorted string, an output overvoltage condition, or an over temperature condition. If used, this pin should be loaded with a high impedance stage as specified in the Operating Characteristics. Do not drive this pin with a voltage, as it will damage the driver.



## ONBOARD PWM DIMMING



Graph 1

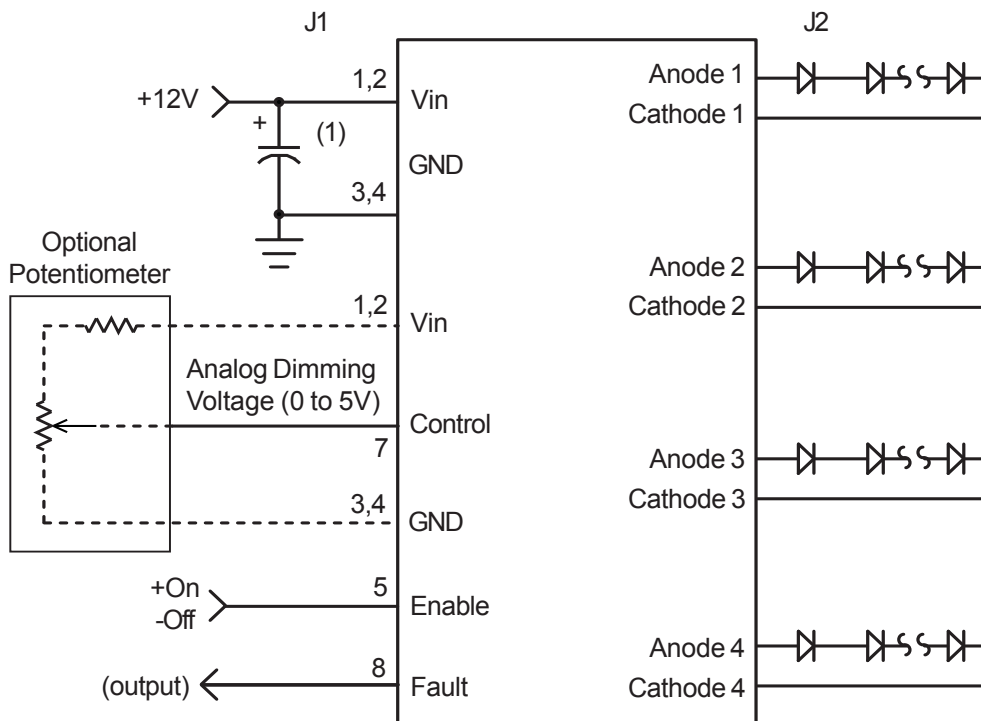


Figure 1

- (1) Low ESR type input by-pass capacitor (10 uF - 220 uF) may be required to reduce reflected ripple and to improve power supply response.



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