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SFD2EB4006F



## Specifications and Applications Information

03/21/11

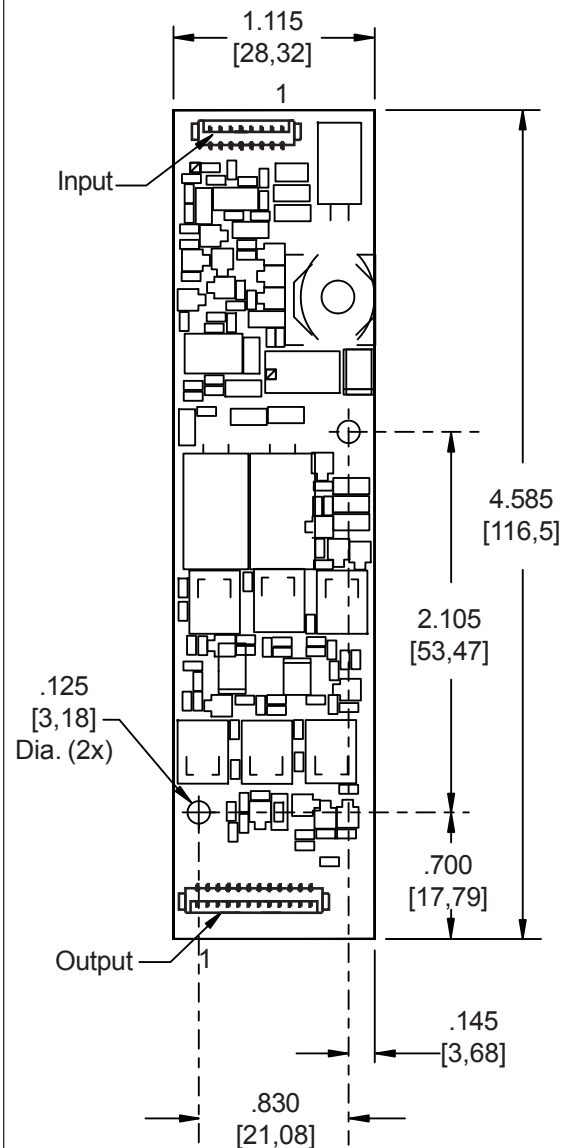
### Smart Force LED Driver

The ERG *Smart Force Series* of LED Drivers are specifically designed for applications which require wide dimming and LCD brightness stability over a wide input voltage range. The SFD2EB4006F is designed to provide backlight power for the Optrex T-55563D104J-LW-A-ABN display.

Designed, manufactured and supported within the USA, the SFD2E features:

- ✓ 10 mm or less in height
- ✓ Wide input voltage range
- ✓ Constant LED current
- ✓ External dimming or on-board dimming
- ✓ High dimming ratio
- ✓ Soft start
- ✓ One year warranty

#### Package Configuration



PCB components are shown for reference only. Actual product may differ from that shown.

#### Connectors

| Input Connector  | Output Connector*  |
|--|--|
| Molex<br>53261-0871  | Molex<br>53261-1271  |
| J1-1 Vin(+)<br>J1-2 Vin(+)<br>J1-3 Vin(+)<br>J1-4 GND<br>J1-5 GND<br>J1-6 GND<br>J1-7 Enable<br>J1-8 Control | J2-1 Cathode 1    J2-7 Cathode 4<br>J2-2 Anode 1     J2-8 Anode 4<br>J2-3 Cathode 2   J2-9 (do not use)<br>J2-4 Anode 2     J2-10 (do not use)<br>J2-5 Cathode 3   J2-11 (do not use)<br>J2-6 Anode 3     J2-12 (do not use) |
|  | * Requires harness:<br>ERG part number H15008152F recommended  |

Mass: 18 grams typ.



**Absolute Maximum Ratings**

| Rating                | Symbol       | Value         | Units |
|-----------------------|--------------|---------------|-------|
| Input Voltage Range   | $V_{in}$     | -0.3 to +20.0 | Vdc   |
| Storage Temperature   | $T_{stg}$    | -40 to +85    | °C    |
| Enable Input Voltage  | $V_{Enable}$ | 0 to $V_{in}$ | Vdc   |
| Control Input Voltage | $V_{PWM}$    | 0 to +5.0     | Vdc   |

**Operating Characteristics**

Unless otherwise noted  $V_{in} = 12.00$  Volts dc and  $T_a = 25^{\circ}\text{C}$ .

| Characteristic                         | Symbol       | Min   | Typ   | Max   | Units |
|--|--------------|-------|-------|-------|-------|
| Input Voltage                          | $V_{in}$     | +10.8 | +12.0 | +15.0 | Vdc   |
| Component Surface Temperature (Note 1) | $T_s$        | -40   | -     | +80   | °C    |
| Peak Inrush Current (Note 2)           | $I_{peak}$   | -     | 1.1   | -     | Adc   |
| Input Current                          | $I_{in}$     | 0.71  | 0.84  | 0.97  | Adc   |
| LED String Voltage                     | $V_{LED}$    | 19    | -     | 35    | Vdc   |
| Efficiency (Note 3)                    | $\eta$       | -     | 82    | -     | %     |
| Output Current (per string)            | $I_{out}$    | 75    | 80    | 83    | mAdc  |
| <b>Enable Pin</b>                      |              |       |       |       |       |
| Turn-on Threshold                      | $V_{thon}$   | -     | -     | 2.0   | Vdc   |
| Turn-off Threshold                     | $V_{thoff}$  | 0.8   | -     | -     | Vdc   |
| Enable Input Impedance (Note 4)        | $R_{Enable}$ | -     | 5.0   | -     | kOhms |
| <b>Control Pin</b> (Notes 5,6)         |              |       |       |       |       |
| Full-on Threshold                      | $V_{thon}$   | -     | 1.0   | -     | Vdc   |
| Full-off Threshold                     | $V_{thoff}$  | -     | 4.5   | -     | Vdc   |
| Control Input Bias Current             | $I_{Cbias}$  | -     | -     | 10    | uA    |
| Frequency                              | $F_{PWM}$    | -     | 245   | -     | Hz    |

Specifications subject to change without notice.

- Note 1 Surface temperature must not exceed  $80^{\circ}\text{C}$ .  
 Note 2 Peak inrush occurs over a 1 to 3 ms time period during initial startup.  
 Note 3 Efficiency is calculated using a 26.2V LED string.  
 Note 4 Enable pin input impedance is  $5.0\text{k}\Omega$  to  $2.5\text{V}$ .  
 Note 5 Control pin is internally pulled up above the turn-on threshold.  
 Note 6 Control pin input impedance is  $485\text{k}\Omega$ .



## Application Information

The ERG SFD2EB4006F has been designed to be configured in multiple ways:

### NO DIMMING

- OPERATION: The SFD2E can be configured to operate without dimming by floating the Control (J1-8) pin.
- Pins 1, 2 and 3 of connector J1 must be connected to +Vin, between 10.8 and 15 Vdc. Pins 4, 5 and 6 of connector J1 must be connected to GND.
- Enable Pin (J1-7) must be high for the driver to be on.

### ONBOARD PWM DIMMING

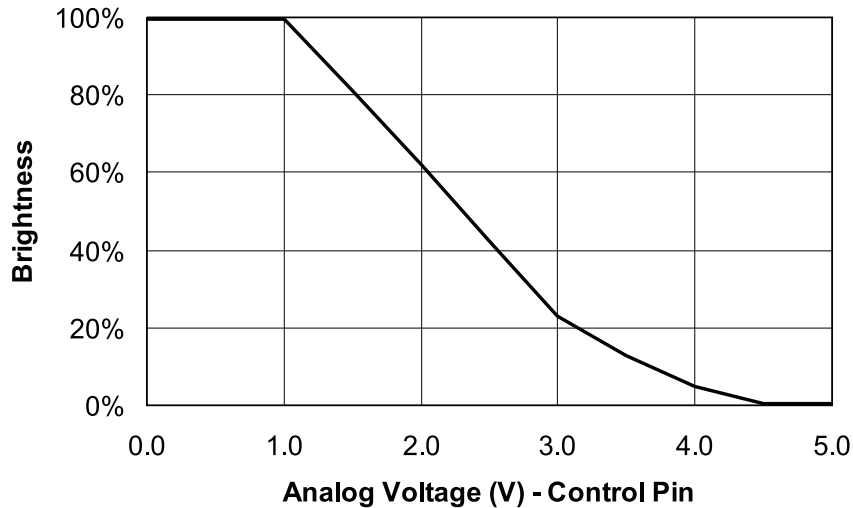
- OPERATION: Onboard PWM configuration as shown in Figure 1 allows the user to control display brightness by controlling the onboard PWM generator. The user is responsible to provide an analog control signal. A minimum pulse width of 80 $\mu$ s is possible with this configuration.
- DIMMING: Dimming is accomplished by applying an analog voltage to the Control Pin (J1-8). Display brightness is modulated by controlling the Control Pin voltage as shown in Graph 1.
- ENABLE/DISABLE: The driver may be enabled or disabled (turned on and off) by applying a DC voltage to the Enable Pin(J1-7). Enable Pin on and off levels are specified in the Operating Characteristics section of the data sheet.
- Pins 1, 2 and 3 of connector J1 must be connected to +Vin, between 10.8 and 15 Vdc. Pins 4, 5 and 6 of connector J1 must be connected to GND.

### EXTERNAL PWM DIMMING

- OPERATION: External PWM configuration as shown in Figure 2 allows the user to control display brightness with an externally generated PWM signal. The user is responsible to provide the PWM signal. A minimum pulse width of 80 $\mu$ s is possible with this configuration.
- DIMMING: Dimming is accomplished by applying a PWM signal to the Enable Pin (J1-7). Enable on and off levels are specified in the Operating Characteristics section of the data sheet. Display brightness is modulated by controlling the PWM duty cycle as shown in Graph 2.
- Pins 1 through 3 of connector J1 must be connected to +Vin, between 10.8 and 15 Vdc. Pins 4 through 6 of connector J1 must be connected to GND.



## ONBOARD PWM DIMMING



Graph 1

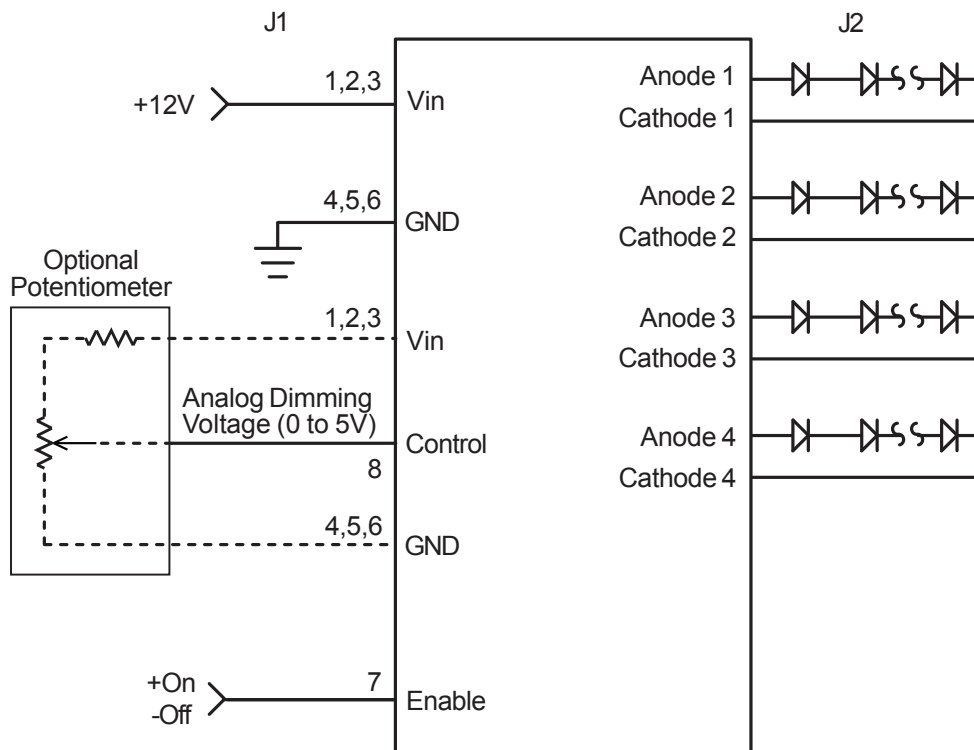
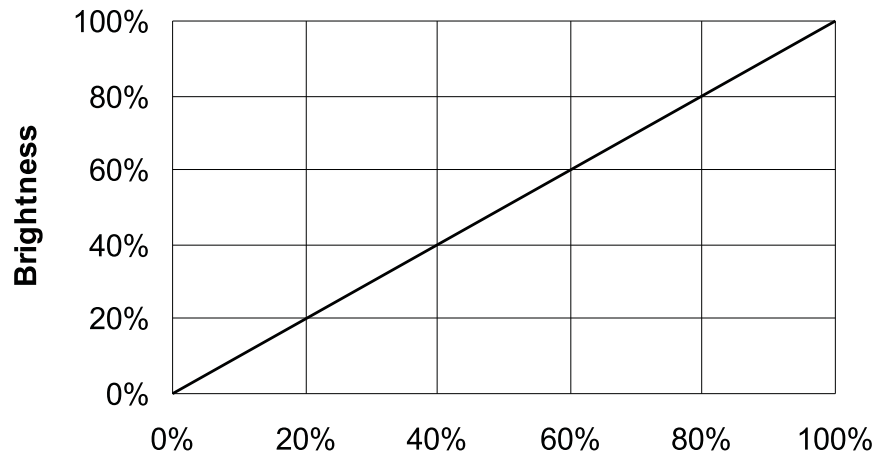


Figure 1



## EXTERNAL PWM DIMMING



**PWM Duty Cycle - Enable Pin <sup>(1)</sup>**

(1) Nonlinear relationship from 0 to 2% duty cycle.

Graph 2

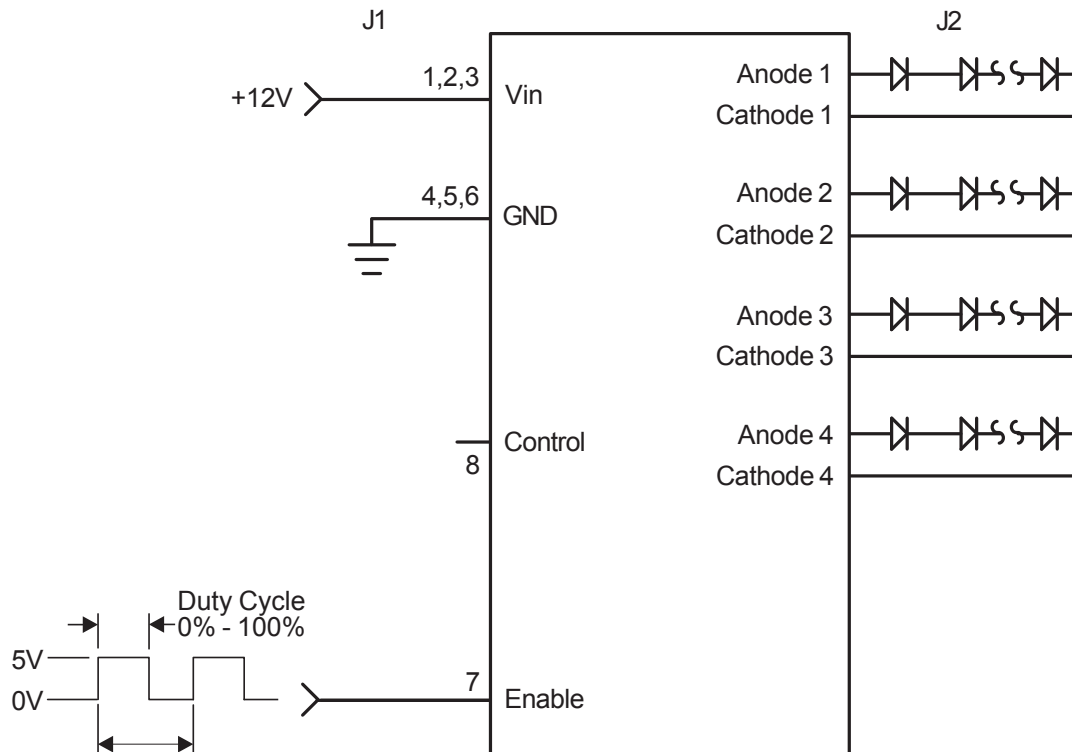


Figure 2



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