Endicott Research Group, Inc.
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8mA23441

Specifications and Applications Information

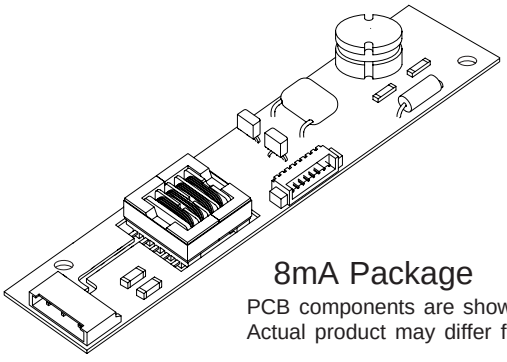
06/16/09 Preliminary

Two Lamp DC to AC Inverter

The ERG 8mA23441 (*8m Class*) low profile dc to ac inverter is specifically designed to power the backlight of the Kyocera TCG104VG2AA-G00 LCD display module to a moderate brightness level from a +5 volt dc source.

This low profile inverter features:

- ✓ Less Than 8 mm in Height
- ✓ LCD Module Specific
- ✓ Display Compatible Output Connector
- ✓ Firm Specifications
- ✓ Application Information
- ✓ Designed, Manufactured and Supported in the USA
- ✓ Custom Input and Output Voltages
- ✓ Flexible System Interface
- ✓ Notebook Display Head Compatible

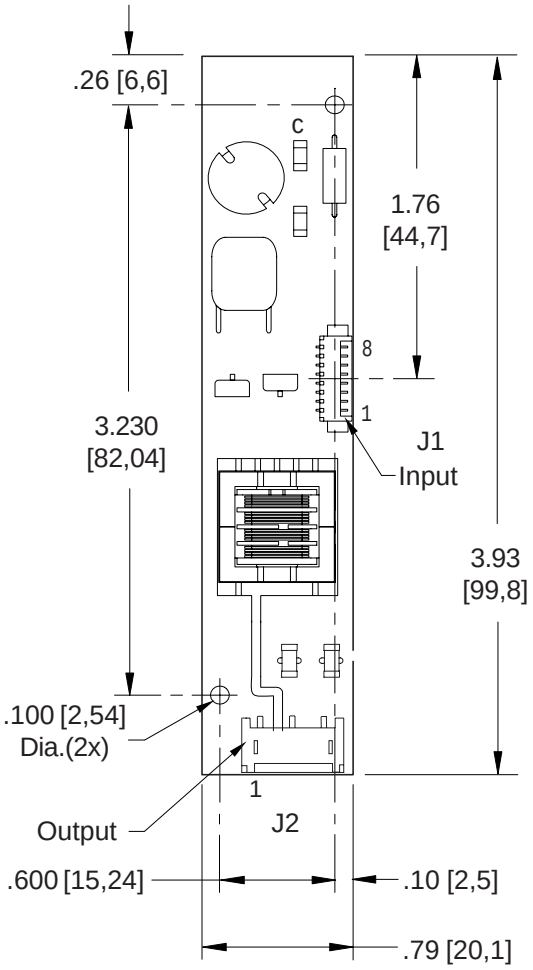


8mA Package

PCB components are shown for reference only. Actual product may differ from that shown.

Connectors	
Input J1 Molex 53261-0871	Output J2 JST SM03(4.0)B-BHS-1-TB

Package Configuration



PCB components are shown for reference only. Actual product may differ from that shown.

Pin Descriptions	
J1-1 +Vin J1-2 +Vin J1-3 GND J1-4 GND J1-5 Enable * J1-6 N/C J1-7 N/C J1-8 GND * Valid only with "C" jumper (JP1) removed	J2-1 ACreturn J2-2 ACout J2-3 ACout

Absolute Maximum Ratings

Rating	Symbol	Value	Units
Input Voltage Range	V_{in}	-0.3 to +5.5	Vdc
Storage Temperature	T_{stg}	-40 to +85	°C

Operating Characteristics

With a load simulating the referenced display and lamp warm-up of 5 minutes.
Unless otherwise noted Vin = 5.00 Volts dc and Ta = 25°C.

Characteristic	Symbol	Min	Typ	Max	Units
Input Voltage	V_{in}	+4.50	+5.00	+5.25	Vdc
Component Surface Temperature (note 1)	T_s	-20	-	+80	°C
Input Current (note 2)	I_{in}	-	1.24	1.40	Adc
Operating Frequency	F_o	38	43	48	kHz
Minimum Output Voltage (note 3)	V_{out} (min)	1400	-	-	Vrms
Efficiency	η	-	82	-	%
Output Current (per lamp)	I_{out}	-	5.0	-	mArms
Output Voltage	V_{out}	-	510	-	Vrms
Enable Pin Input Current Requirement (notes 4,5,6)	I_{Enable}	-	15	-	mAdc

Specifications subject to change without notice.

(Note 1) Surface temperature must not exceed 80 degrees C; thermal management actions may be required.
(Note 2) Input current in excess of maximum may indicate a load/inverter mismatch condition, which can result in reduced reliability. Please contact ERG technical support.
(Note 3) Provided data is not tested but guaranteed by design.
(Note 4) Required User Enable/Disable Interface Circuit is shown on page 3.
(Note 5) Valid only with “C” jumper (JP1) removed.
(Note 6) With the inverter powered and JP1 is in place, a ground applied to the enable pin J1-5 will open the inverter fuse.

Application Notes:

1) The minimum distance from high voltage areas of the inverter to any conductive material should be .12 inches per kilovolt of starting voltage.
2) Mounting hardware to be non-conductive.
3) Open framed inverters should not be used in applications at altitudes over 10,000 feet.
4) Contact ERG for possible exceptions.

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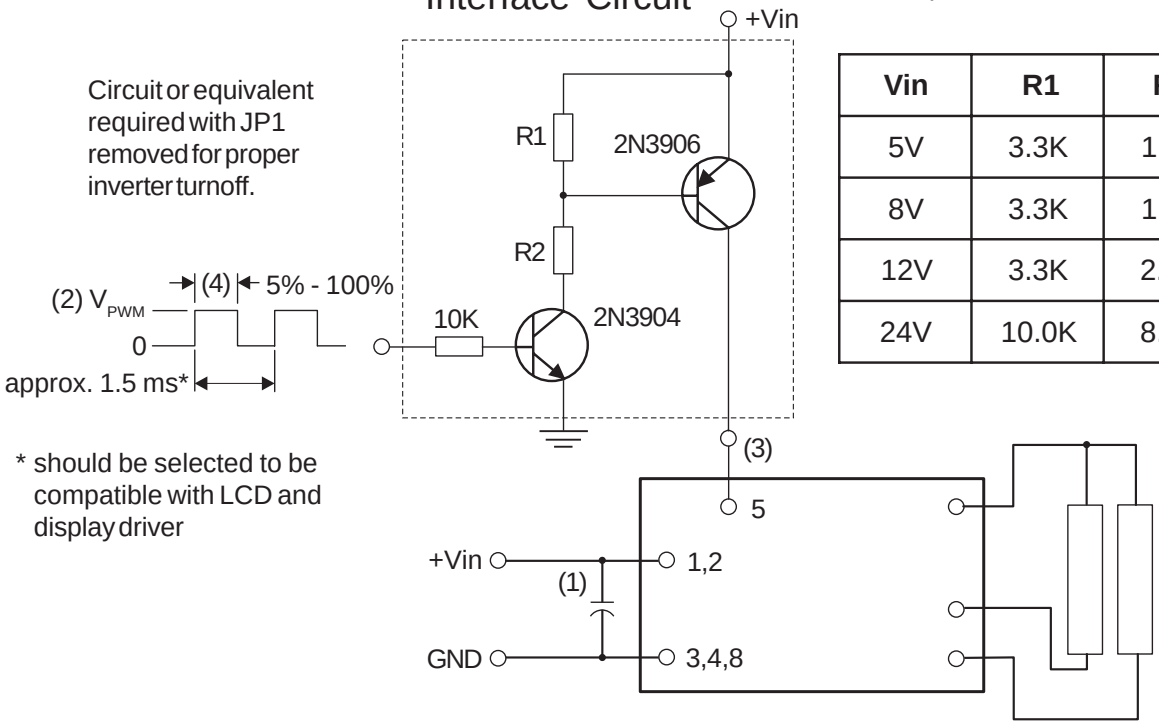
PWM Dimming

(Valid only with JP1 removed)

Required User Enable/Disable Interface Circuit



Circuit or equivalent required with JP1 removed for proper inverter turnoff.

* should be selected to be compatible with LCD and display driver

With JP1 in place, a ground applied to the enable pin J1-5 will open the inverter fuse.

Vin	R1	R2
5V	3.3K	1.5K
8V	3.3K	1.8K
12V	3.3K	2.2K
24V	10.0K	8.2K

(1) Low ESR type input by-pass capacitor (22 uF - 100 uF) may be required to reduce reflected ripple.
(2) V_{PWM} from 2.4V to less than or equal to +Vin.
(3) Full brightness without PWM control requires that pin 5 be tied to +Vin. Pin 5 must be at 0V to turn off.
(4) Duty Cycle 5% - 100%.