



Endicott Research Group, Inc.

2601 Wayne St., Endicott, NY 13760

607-754-9187 Fax 607-754-9255

http://www.ergpower.com

10m053420

Specifications and Applications Information

04/07/10

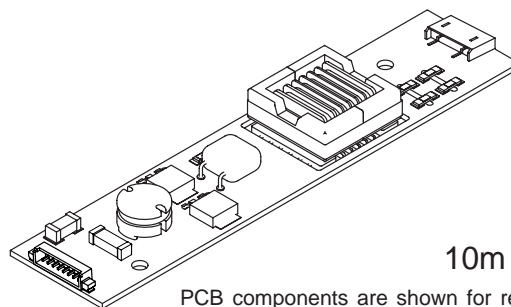
10m Class
Single Lamp
DC to AC Inverter

The ERG 10m053420 (10m Class) low profile dc to ac inverter is specifically designed to power the following display module(s) to a moderate brightness level from a +5 volt dc power supply:

- Kyocera TCG057QV1AD-G00
- Kyocera TCG057QV1DC-G50

This low profile inverter features:

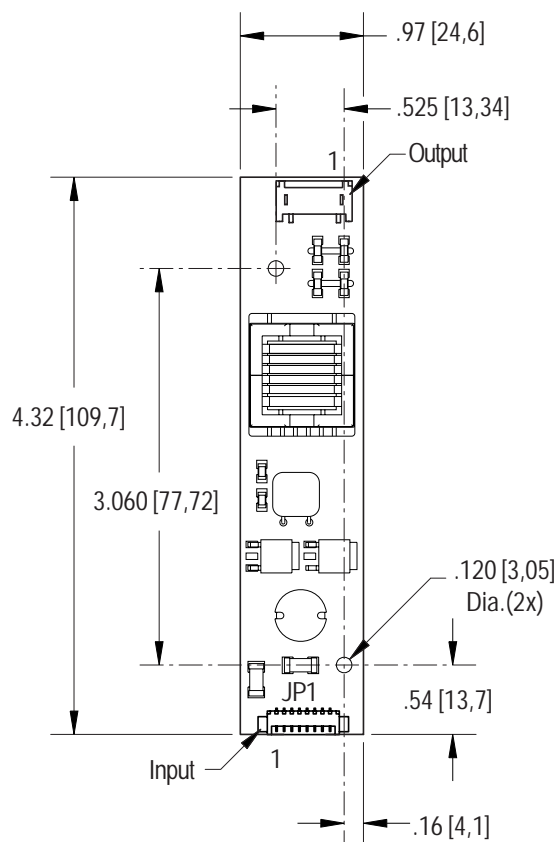
- ✓ Less Than 10 mm in Height
- ✓ LCD Module Specific
- ✓ Display Compatible Output Connector
- ✓ Firm Specifications
- ✓ Application Information
- ✓ Designed, Manufactured and Supported in the USA
- ✓ Custom Input and Output Voltages
- ✓ Flexible System Interface



10m Package

PCB components are shown for reference only. Actual product may differ from that shown.

Package Configuration



Mass: 22 grams

PCB components are shown for reference only. Actual product may differ from that shown.

Connectors

| Input Connector | | Output Connector | |
|-------------------------------|----------|----------------------------|----------|
| Molex 53261-0871 | | JST SM02(8.0)B-BHS-1-TB | |
| J1-1,2 | +Vin | J2-1 | ACout |
| J1-3,4 | GND | J2-2 | ACreturn |
| J1-5 | Enable * | | |
| J1-6,7,8 | N/C | | |
| * Valid only with JP1 removed | | | |

Absolute Maximum Ratings

| Rating | Symbol | Value | Units |
|---------------------|-----------|---------------|-------|
| Input Voltage Range | V_{in} | -0.3 to +5.50 | Vdc |
| Storage Temperature | T_{stg} | -40 to +85 | °C |

Operating Characteristics

With a load simulating the referenced display and lamp warm-up of 5 minutes.
Unless otherwise noted $V_{in} = 5.00$ Volts dc and $T_a = 25^{\circ}\text{C}$

| Characteristic | Symbol | Min | Typ | Max | Units |
|--|-----------------------|-----------------------------|----------------|-----------------------|-------|
| Input Voltage | V_{in} | +4.75 | +5.00 | +5.25 | Vdc |
| Component Surface Temperature (note 1) | T_s | -20 | - | +80 | °C |
| Input Current (note 2) | I_{in} | - | 0.72 | 0.83 | Adc |
| Operating Frequency | F_o | 36 | 41 | 46 | kHz |
| Minimum Output Voltage (note 3) | $V_{out}(\text{min})$ | 2200 | - | - | Vrms |
| Efficiency | η | - | 76 | - | % |
| Output Current (per lamp) | I_{out} | - | 4.0 | - | mArms |
| Output Voltage | V_{out} | - | 685 | - | Vrms |
| Enable Pin Input Current Requirement (notes 4,5,6) | I_{Enable} | - | 6 | - | mAdc |
| Enable Pin Input Voltage Requirement (notes 4,5,6) | V_{Enable} | Off 0 or Floating | On 5 | On V_{in} | Vdc |

Specifications subject to change without notice.

(Note 1) Surface temperature must not exceed 80 degrees C; thermal management actions may be required.

(Note 2) Input current in excess of maximum may indicate a load/inverter mismatch condition, which can result in reduced reliability. Please contact ERG technical support.

(Note 3) Provided data is not tested but guaranteed by design.

(Note 4) Required User Enable/Disable Interface Circuit is shown on page 3.

(Note 5) Valid only with JP1 removed.

(Note 6) With the inverter powered and JP1 is in place, a ground applied to the enable pin J1-5 will open the inverter fuse.

Application Notes:

- 1) The minimum distance from high voltage areas of the inverter to any conductive material should be .12 inches per kilovolt of starting voltage.
- 2) Mounting hardware to be non-conductive.
- 3) Open framed inverters should not be used in applications at altitudes over 10,000 feet.
- 4) ACreturn should be left floating, not grounded.
- 5) Contact ERG for possible exceptions.



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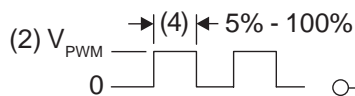
Made in USA

PWM Dimming

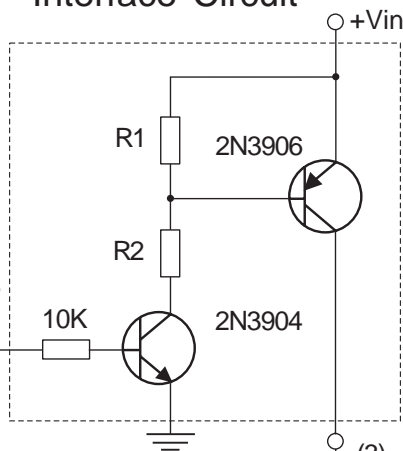
(Valid only with JP1 removed)

Circuit or equivalent required with JP1 removed for proper inverter turnoff.

PWM frequency 100-300 Hz should be selected to be compatible with LCD and display driver.

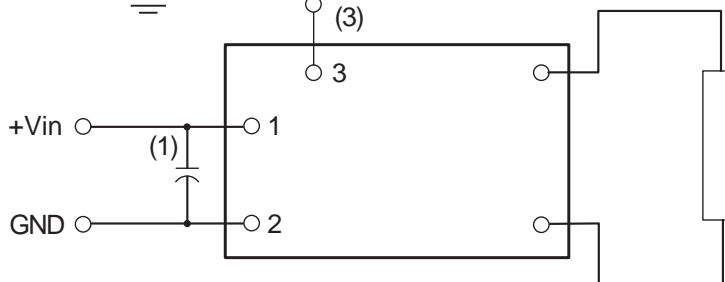


Required User Enable/Disable Interface Circuit



With JP1 in place, a ground applied to the enable pin J1-5 will open the inverter fuse.

| Vin | R1 | R2 |
|-----|-------|------|
| 5V | 3.3K | 1.5K |
| 8V | 3.3K | 1.8K |
| 12V | 3.3K | 2.2K |
| 24V | 10.0K | 8.2K |



- (1) Low ESR type input by-pass capacitor (22 μ F - 100 μ F) may be required to reduce reflected ripple.
- (2) V_{PWM} from 2.4V to less than or equal to +Vin.
- (3) Full brightness without PWM control requires that pin 5 be tied to +Vin. Pin 5 must be at 0V to turn off.
- (4) Duty Cycle 5% - 100%.



Endicott Research Group, Inc. (ERG) reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by ERG is believed to be accurate and reliable. However, no responsibility is assumed by ERG for its use.